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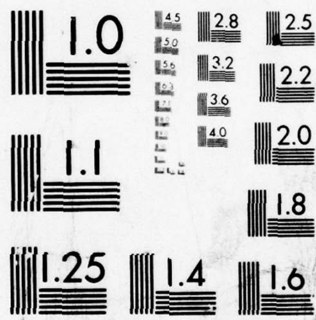
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TECHNICAL REPORT NO. 2

SEPTEMBER 1979

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PREPARED FOR

OFFICE OF NAVAL RESEARCH
ARLINGTON, VIRGINIA

TRW

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA 90278

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A design for a low noise monolithic X-band preamplifier has been developed based on TRW's FET computer model. The design utilizes a single ended configuration, FET devices structured and biased for minimum noise, and microelectronic spiral rectangular inductors.

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CONTENTS

ILLUSTRATIONS

1.0 INTRODUCTION

During the initial phase of this contract, TRW developed a computer model for GaAs Microwave Field-Effect Transistors, in order to study the noise and gain properties of such devices for different channel doping densities and geometry configurations. This model has proven to be accurate when compared against measured results of noise figure, S parameters, and temperature effects on noise figure of FET devices.

At the present, TRW has made use of this computer model in designing a low noise integrated preamplifier to operate at X-band. The theoretical design of this amplifier is the subject of the present report.

2.0 PERFORMANCE GOALS

As stated in the technical and cost proposal (TRW No. 32153, June 1977, page 1-1) the performance goals for the preamplifier can be summarized as follows:

- Gain — 30 dB at 10 GHz
- Noise Figure — <3.0 dB at 10 GHz
- DC Power Consumption — <500 mW
- Frequency Response — 8.0 to 11.0 GHz

3.0 SELECTION CRITERIA FOR THE FET DEVICES

The necessary requirements for the FET devices to be used on the preamplifier design are discussed below.

3.1 Low Noise Figure

For a multi-stage single-ended amplifier, the overall noise figure is given by the well known Friis' formula

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \frac{NF_4 - 1}{G_1 G_2 G_3} + \ldots \qquad (3\text{-}1)$$

where NF_1, G_1 are the noise figure and gain of the first stage; NF_2, G_2 those of the second stage, and so forth. For large $G_1 G_2$, this equation can be approximated to

$$NF \simeq NF_1 + \frac{NF_2 - 1}{G_1} \qquad (3\text{-}2)$$

If $NF_1 = NF_2$, one can solve for NF_1 from equation (3-2) and obtain

$$NF_1 = \frac{1 + G_1 NF}{1 + G_1} \qquad (3\text{-}3)$$

From equation (3-3) for a gain at 10 GHz of 5 dB, the required noise figure, NF_1, is estimated to be 2.5 dB. Allowing 0.5 dB for losses due to input mismatch, plus insertion loss of input matching network, the minimum upper bound for the noise figure of the FET devices is set at 2.5 dB - 0.5 dB = 2.0 dB; therefore

$$NF_1 \leq 2 \text{ dB at 10 GHz} \qquad (3\text{-}4)$$

3.2 High Associated Gain

It follows from the discussion of the previous paragraph that the required gain for the FET devices with their input terminated in a minimum noise source impedance should be greater than 5 dB; therefore

$$G_1 \geq 5 \text{ dB at 10 GHz} \qquad (3\text{-}5)$$

3.3 Reasonable Input and Output Impedances

Since FET devices have typically high input and output impedances, it is often necessary to use matching sections of 4 or 5 elements in order to transform high impedance levels to 50 ohms. Monolithic implementations of reactive matching elements are typically relatively low Q, making it difficult to match to devices having very high reflection coefficients. Thus it is desirable for the FET's to have

$$\begin{aligned} |S_{11}| &< 0.9 \qquad |\angle S_{11}| > 20^\circ \\ |S_{22}| &< 0.9 \qquad |\angle S_{22}| > 20^\circ \end{aligned} \qquad (3\text{-}6)$$

A device that closely fulfills the requirements specified by (3-4), (3-5) and (3-6) as calculated by the TRW FET computer model has the following geometry, doping densities and resistivities.

Gate length	1 μm
Channel depth	0.34 μm
Device width	360 μm
Gate-source separation	1 μm
Gate-drain separation	1 μm

Doping under source contact	5×10^{17} cc^{-3}
Doping under drain contact	5×10^{17} cc^{-3}
Doping under gate contact	4×10^{16} cc^{-3}
Doping between gate and source contact	4×10^{16} cc^{-3}
Doping between gate and drain contact	4×10^{16} cc^{-3}
Specific contact resistivity of source	1×10^{-6} $\Omega\text{-cm}^2$
Specific contact resistivity of drain	1×10^{-6} $\Omega\text{-cm}^2$
Sheet resistance of all metal contacts	0.06 Ω / □
Number of gate contact points	2

This device under the biasing conditions

V_{DD} = 3.0 volts

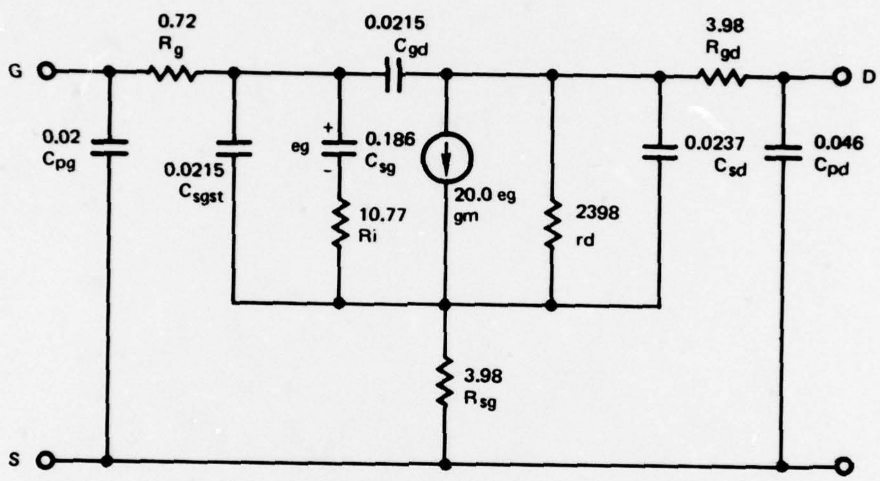
V_{GG} = -0.8 V_p = -2.0 volts

I_d = 8.4 mA

has an equivalent circuit shown in Figure 3.1, and the following set of S parameters.

F (GHz)	S_{11}	S_{21}	S_{12}	S_{22}
8	$0.889\angle{-65.0}$	$1.414\angle{125.1}$	$0.084\angle{48.5}$	$0.915\angle{-28.9}$
9	$0.871\angle{-71.1}$	$1.345\angle{119.8}$	$0.090\angle{44.8}$	$0.908\angle{-32.0}$
10	$0.855\angle{-76.7}$	$1.278\angle{114.7}$	$0.095\angle{41.4}$	$0.902\angle{-35.0}$
11	$0.839\angle{-81.9}$	$1.213\angle{110.0}$	$0.099\angle{38.3}$	$0.896\angle{-37.9}$

The noise figure, optimum source reflection coefficient for minimum noise, the associated gain, and the noise resistance are



- ALL RESISTOR VALUES ARE IN OHMS
- ALL CAPACITOR VALUES ARE IN P.F.
- TRANSCONDUCTANCE OF VOLTATE – CONTROLLED CURRENT SOURCE IS IN MMHOS

Figure 3-1. FET equivalent circuit model

F (GHz)	NF	Γs opt	Associated Gain (dB)	R_n (Ω)
8	1.78	$0.843\underline{\lvert 26.5}$	5.38	4.7
9	1.96	$0.828\underline{\lvert 29.7}$	4.82	4.7
10	2.14	$0.813\underline{\lvert 32.8}$	4.34	4.7
11	2.30	$0.799\underline{\lvert 35.9}$	3.90	4.7

In the circuit model of the FET device, the components are defined as follows:

R_g = Gate metalization resistance

R_i = Gate charging resistance: proportional to transit time of carriers through the channel and inversely proportional to gate length and source to gate capacitance

rd = Drain resistance; or rate of change of drain current to drain-source voltage for a fixed gate to source voltage

R_{gd} = Drain parasitic resistance; this resistance is the total of channel resistance between gate and drain contacts, plus the metal to semiconductor interface resistance plus the metalization resistance of the drain contact

R_{sg} = Source parasitic resistance: evaluated in the same manner as R_{gd}

C_{pg} = Gate pad capacitance: proportional to the area of the gate pad, inversely proportional to the distance between the pad and the ground plane, plus fringing effects

C_{sgst} = Static source-gate capacitance, due to interelectrode capacitance between parallel strips immersed in a dielectric half-space

C_{sg} = Source-gate capacitance: or rate of change of the free charge on the gate electrode with respect to the gate bias voltage when the drain potential is held fixed

C_{gd} = Gate-drain capacitance: evaluated in the same manner as C_{sgst}

C_{sd} = Source-drain capacitance: evaluated in the same manner as C_{sgst}

C_{pd} = Drain pad capacitance: evaluated in the same manner as C_{pg}

For the mathematical equations used in the calculation of the circuit elements of Figure 3.1, reference is made to "TRW Monolithic Microwave Preamplifier Technical Report, pages 2-10 to 2-14 and 6-1 to 6-5, October 1978."

4.0 SELECTION CRITERIA FOR THE AMPLIFIER CONFIGURATION

Three basic approaches can be considered for the amplifier configuration: a single-ended multiple stage design, a balanced amplifier input stage followed by a single-ended amplifier chain, and a cascade connection of several balanced stages.

4.1 Single Ended Amplifier

This configuration has the block diagram shown in Figure 4.1.

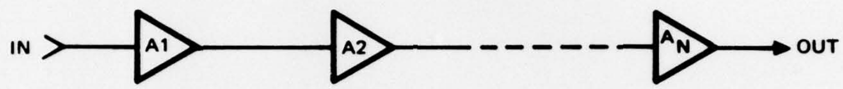


Figure 4.1 Single-ended amplifier block diagram.

The main advantage of this approach is the simplicity of the design, which makes it the optimum candidate for a first attempt to build a complete low noise preamplifier on a chip. The main disadvantage is a relatively high input VSWR.

4.2 Balanced Amplifier

The block diagram for this configuration is shown in Figure 4.2.

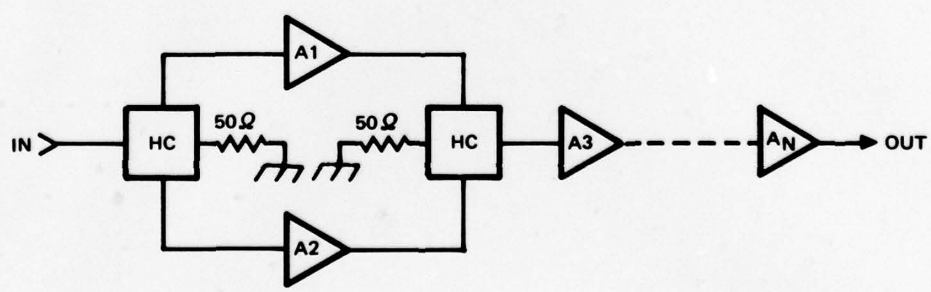


Figure 4.2 Balanced amplifier block diagram.

The main advantage of this configuration is the low input VSWR that can be obtained throughout the frequency range of interest. The main disadvantage is the added complexity of the system due to the hybrid couplers.

4.3 Cascade Connection of Balanced Stages

The block diagram for this configuration is shown in Figure 4.3.

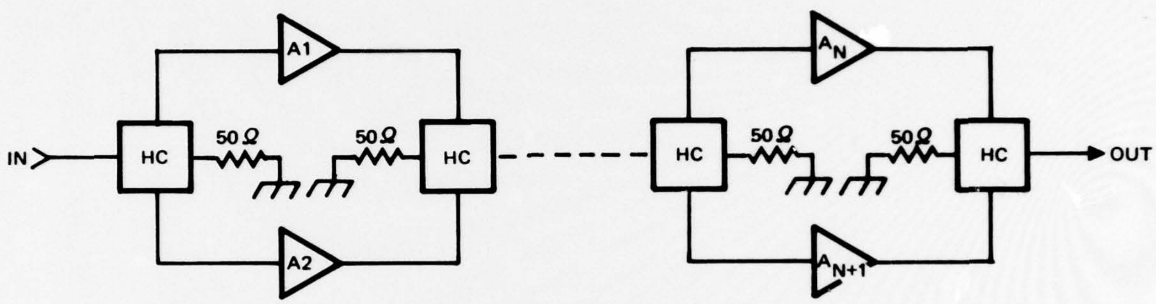


Figure 4.3 Block diagram of a cascade connection of balanced stages.

The main advantage of this configuration is again the low input and interstage VSWR that can be obtained throughout the frequency range of interest. The main disadvantage is the added complexity of the system due to the hybrid couplers and the number of active FET stages required; also, the DC power consumption is almost double that of the single-ended configuration.

5.0 AMPLIFIER DESIGN

5.1 Determining the Number of Stages

Since the associated gain at 11.0 GHz of the device selected in section 3.0 is 3.9 dB, to obtain an overall gain of 30 dB we require

$$\text{Number of Stages} = \frac{30\ \text{dB}}{3.9\ \text{dB}} = 7.4 \Rightarrow 8\ \text{stages} \qquad (5\text{-}1)$$

5.2 Determining the Expected Power Consumption

At biasing conditions of $V_{DD} \simeq 3$ volts and $I_d \simeq 8.4$ mA, the total power consumption of an 8 stage amplifier is

$$P_{dc} = (3.0 \text{ volts}) \ (8 \times 8.4 \text{ mA}) = 201.6 \text{ mW} \qquad (5\text{-}2)$$

which is well below the initial specification of 500 mW.

5.3 Stability Analysis of the First Stage When is Being Driven by a Generator with Optimum Noise Source Impedance.

From the S parameters of the device specified in Section 3.0, the stability factor, K, can be calculated from the equation[1]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}\,S_{21}|} \qquad (5\text{-}3)$$

where

$$\Delta = S_{11}\,S_{22} - S_{12}\,S_{21} \qquad (5\text{-}4)$$

Evaluating (5-3) throughout the frequency range of interest gives

F (GHz)	K
8	0.226
9	0.267
10	0.297
11	0.328

and since $K < 1$ in this frequency range, the device is potentially unstable. The regions of instability on the Smith Chart are the areas inside the input and output stability circles whose radii are given by the expressions[2]

$$\rho_{is} = \frac{|S_{12}\,S_{21}|}{\left||S_{11}|^2 - |\Delta|^2\right|} \quad \text{(input)} \qquad (5\text{-}5)$$

$$\rho_{os} = \frac{|S_{12}\,S_{21}|}{\left||S_{22}|^2 - |\Delta|^2\right|} \quad \text{(output)} \qquad (5\text{-}6)$$

and the centers of these circles are given by

$$\ell_{is} = \frac{(S_{11} - S_{22}^{*}\,\Delta)^{*}}{|S_{11}|^2 - |\Delta|^2} \quad \text{(input)} \qquad (5\text{-}7)$$

$$\ell_{os} = \frac{(S_{22} - S_{11}^* \Delta)^*}{|S_{22}|^2 - |\Delta|^2} \quad \text{(output)} \tag{5-8}$$

Evaluation of equations (5-5) to (5-8) over the frequency range of interest for the device under discussion gives the following results

Input Stability Circles (I.S.C.)

F (GHz)	Radius	Center Mag. <Angle
8	1.09	$1.64\angle 102.48$
9	1.09	$1.67\angle 107.58$
10	1.06	$1.66\angle 111.90$
11	1.01	$1.64\angle 115.50$

Output Stability Circles (O.S.C)

F (GHz)	Radius	Center Mag. <Angle
8	0.86	$1.46\angle 60.88$
9	0.66	$1.35\angle 58.11$
10	0.62	$1.32\angle 58.50$
11	0.55	$1.29\angle 58.93$

Thus, source and local reflection coefficients that lie outside these circles must be chosen for stable operation. Since the source reflection coefficient has already been predetermined for minimum noise operation, it is firstly verified that it lies outside the input stability circle; this happens to be the case for all frequencies between 8 and 11 GHz. The corresponding load reflection coefficient for maximum power transfer is calculated according to the expression[3]

$$\Gamma_L = \left(\frac{S_{22} - \Delta\, \Gamma_S \text{ opt}}{1 - S_{11}\, \Gamma_S \text{ opt}} \right)^* \tag{5-9}$$

For the chosen FET expression, (5-9) yields

F (GHz)	Γ_L Mag. <Angle
8	$0.754\underline{\lvert 28.85}$
9	$0.756\underline{\lvert 32.04}$
10	$0.759\underline{\lvert 34.98}$
11	$0.762\underline{\lvert 37.90}$

and these reflection coefficients must also be verified to be outside the output stability circle; this also happens to be the case throughout the frequency range of interest. A plot of such verifications from 8 to 11 GHz is shown in Figure 5.1. For unconditional stability, the input reflection coefficient of the FET with its output terminal in a reflection coefficient Γ_L, must have a magnitude less than unity: i.e., $|S_{11}'|<1$; the expression to be evaluated in this case is[3]

$$S_{11}' = \frac{S_{11} - \Delta\Gamma_L}{1 - S_{22}\,\Gamma_L} \tag{5-10}$$

which gives

F (GHz)	S_{11}' Mag. <Angle
8	$0.974\underline{\lvert 57.67}$
9	$0.965\underline{\lvert 57.36}$
10	$0.959\underline{\lvert 57.50}$
11	$0.953\underline{\lvert 57.60}$

thus, the device is unconditionally stable when driven by its optimum noise source impedance and terminated in the corresponding load for maximum power transfer.

5.4 Design of the Input Matching Network

The input matching network, M_1, must provide the FET with its optimum noise source reflection coefficient when its input is terminated in 50 ohms; this is shown in Figure 5.2.

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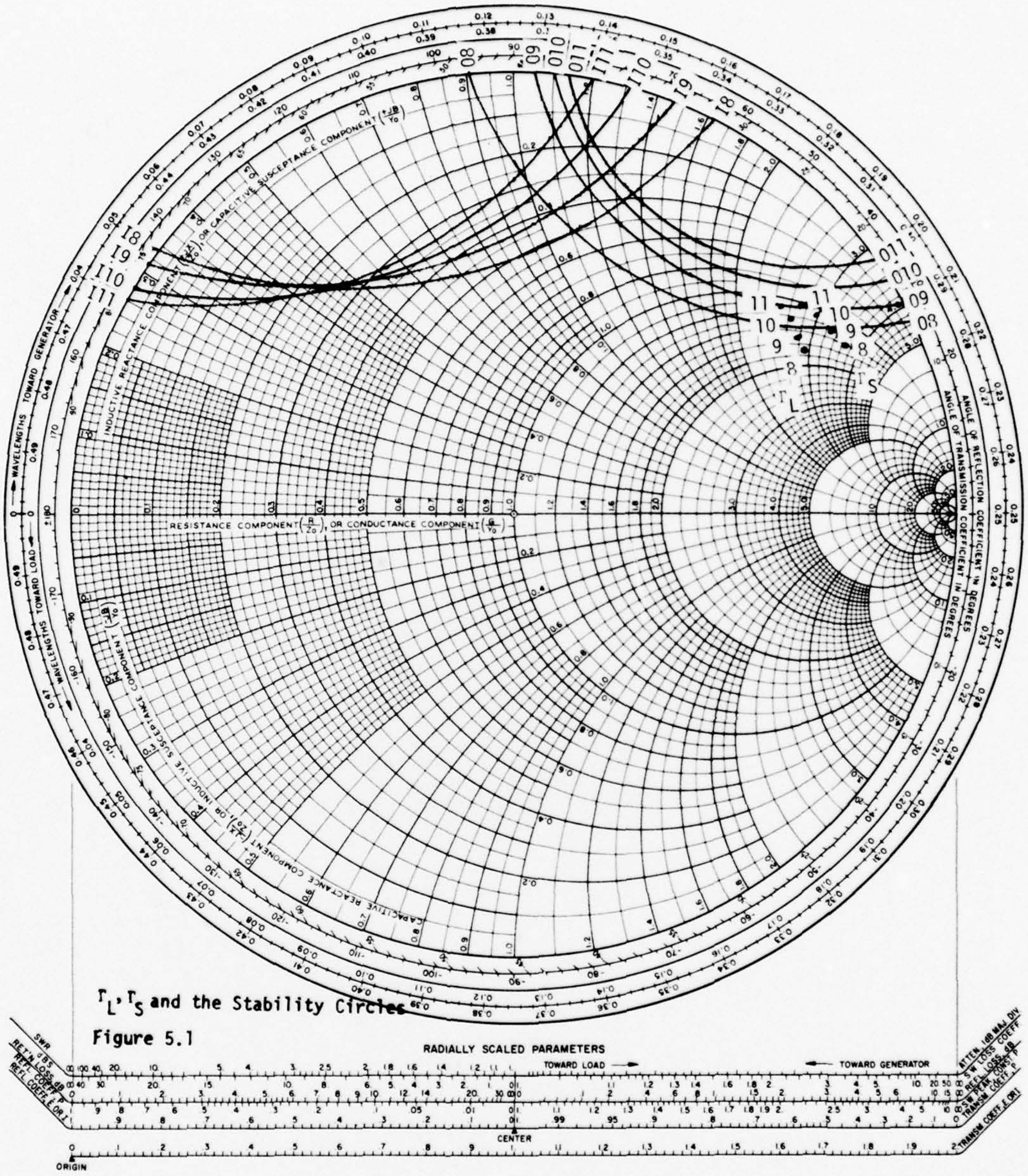


Γ_L, Γ_S and the Stability Circles

Figure 5.1

Figure 5.2 Block diagram of the input matching network M1.

Furthermore, it must contain a DC path to bias the gate of the device and must provide DC isolation to the input signal; in order to keep the noise sources to a minimum, M_1 must be resistor-free. The selected input matching section that fulfills these requirements has the configuration shown in Figure 5.3.

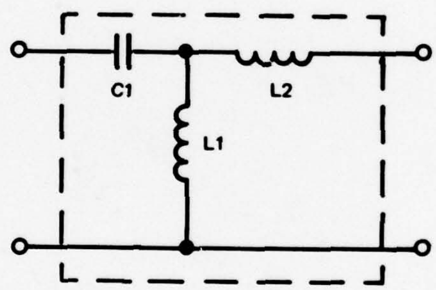


Figure 5.3 Input matching network M1.

The synthesis is performed by minimizing the input reflection coefficient when the network, M_1, is terminated at its output with a reflection coefficient Γ_S^* opt; at 10 GHz Γ_S^*opt has the equivalent circuit shown in Figure 5.4.

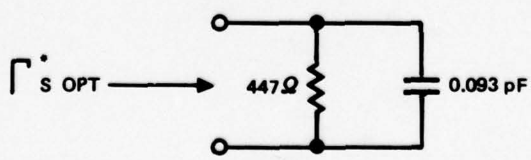


Figure 5.4 Γ_S opt equivalent circuit.

Thus, computer optimization routines give for the component elements the values

$$C_1 = 0.4 \text{ pF}$$
$$L_1 = 1.27 \text{ nH}$$
$$L_2 = 2.02 \text{ nH}$$

which present to the FET the following source reflection coefficients

F (GHz)	Γ_S
8	$0.766\angle 31.0$
9	$0.756\angle 30.7$
10	$0.763\angle 30.6$
11	$0.780\angle 30.4$

These reflection coefficients lie outside the input stability circle. Computation of the associated S_{22}' according to the equation[3]

$$S_{22}' = \frac{S_{22} - \Delta\Gamma_S}{1 - S_{11}\Gamma_S} \qquad (5\text{-}11)$$

gives

F (GHz)	S_{22}'
8	$0.761\angle -31.28$
9	$0.769\angle -33.21$
10	$0.773\angle -35.17$
11	$0.776\angle -37.25$

since $|S_{22}'|<1$, stage 1, is stable for the frequency range 8-11 GHz.

5.5 Design of the Interstage Network Between Stages 1 and 2

The interstage matching network, M_2, must provide the FET of the second stage with its optimum noise source reflection coefficient, as well as providing the FET of the first stage with its optimum load for maximum power transfer. This situation is shown in Figure 5.5.

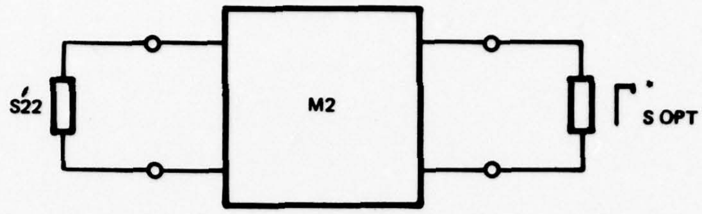


Figure 5.5 Block diagram of network M2.

Also network M_2 must provide DC paths to bias the drain of the first FET and the gate of the second FET, as well as DC isolation between stages 1 and 2; like network M_1, this interstage network must also be resistor-free in order to minimize noise sources.

Present state-of-the-art technology imposes the following constraints on element values at 10 GHz.

	Min.	Max.
Capacitor values (pF)	0.1	10.0
Inductor values (nH)	0.4	10.0
Resistor values (ohms)	0	100 K

The chosen configuration for M_2 is shown in Figure 5.6.

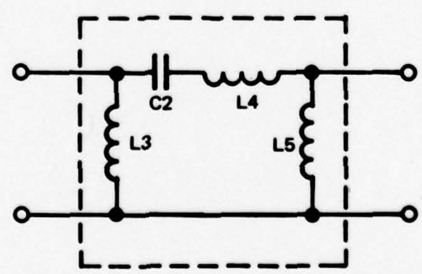


Figure 5.6 Interstage matching network M2.

The synthesis of this network is performed in a manner similar to that for M_1; it is assumed that M_2 is terminated at its output with a reflection coefficient Γ_S^* opt and the input reflection ocefficient is optimized to yield $S_{22}'^*$.

Computer optimization routines gives for the values

$C_2 = 12$ pF

$L_3 = 5.2$ nH

$L_4 = 2.6$ nH

$L_5 = 1.7$ nH

Capacitor C_2 has slightly exceeded the required maximum limit previously established. At the final phase of the design, an attempt will be made during the overall optimization of the amplifier to enforce these maximum and minimum limits of the component values by allowing those components whose values are well within the established range to compensate for the difference. If this attempt is not successful, the slightly exceeded values will be tolerated.

The cascade connection of M_1, stage 1, M_2, stage 2 yields an output reflection coefficient S_{22}' of stage 2 as follows

F (GHz)	S_{22}'
8	$0.88\angle{-45}$
9	$0.81\angle{-41}$
10	$0.81\angle{-41}$
11	$0.83\angle{-42}$

and since $|S_{22}'|<1$, stage 2 is stable for the frequency range 8-11 GHz.

5.6 Design of the Interstage Network Between Stages 2 and 3

This interstage matching network, M_3, need no longer provide an optimum noise source reflection coefficient to the third stage and in order to minimize the number of inductors, resistors can now be introduced to bias the gates of the FET devices; this network, however, must present to the output of the cascade combination of M_1, stage 1, M_2, stage 2, the corresponding $S_{22}'^{*}$ and to the input of stage 3 a source impedance such that stage 3 has adequate gain-slope compensation. The configuration for M_3 is, then, that of Figure 5.7.

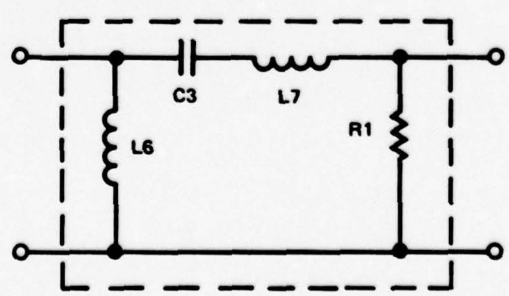


Figure 5.7 Interstage matching network M3.

and the values are synthesized as

$$C_3 = 11.4 \text{ pF}$$

$$R_1 = 10.37 \text{ K}\Omega$$

$$L_6 = 10.7 \text{ nH}$$

$$L_7 = 1.2 \text{ nH}$$

The corresponding S_{22}' of the cascade connection of M_1, stage 1, M_2, stage 2, M_3, stage 3 is

F (GHz)	S_{22}'
8	$0.89\angle{-29}$
9	$0.89\angle{-35}$
10	$0.81\angle{-41}$
11	$0.75\angle{-40}$

and again $|S_{22}'|<1$, which means that stage 3 is stable for the frequency range 8-11 GHz.

5.7 Design of the Remaining Interstage Matching Networks and the Output Matching Section

By following the same procedure as that for M_3, sections M_4, M_5, M_6 and M_7 matching stages 3 and 4, 4 and 5, 5 and 6, 6 and 7 respectively; are synthesized as shown in Figure 5.8.

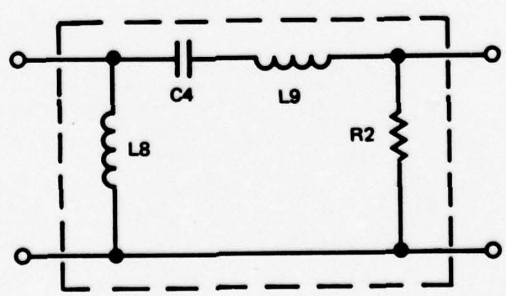


Figure 5.8 Interstage matching network M4, M5, M6 and M7.

with the values

$$C_4 = 11.4 \text{ pF}$$

$$R_2 = 10.37 \text{ K}\Omega$$

$$L_8 = 14.8 \text{ nH}$$

$$L_9 = 1.2 \text{ nH}$$

For section M_8, matching stages 7 and 8, the values become

$$C_4 = 5.5 \text{ pF}$$

$$R_2 = 7.5 \text{ K}\Omega$$

$$L_8 = 14.8 \text{ nH}$$

$$L_9 = 2.7 \text{ nH}$$

The output matching section operates between the resulting S_{22}' of all the eight stages connected in cascade through their respective interstage matching networks, and the 50 ohm load; this last section, M_9, has the configuration shown in Figure 5.9.

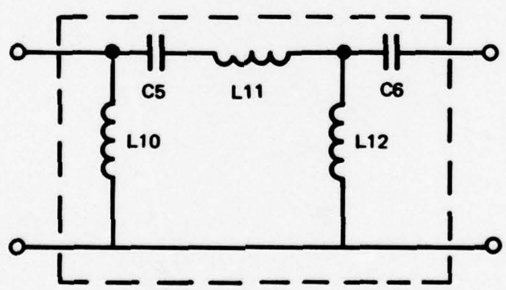


Figure 5.9 Output matching network M9.

with the values synthesized as

$$C_5 = 5.1 \text{ pF}$$

$$C_6 = 6.1 \text{ pF}$$

$$L_{10} = 8.4 \text{ nH}$$

$$L_{11} = 1.9 \text{ nH}$$

$$L_{12} = 0.6 \text{ nH}$$

5.8 Final Optimization Including Losses

Since many of the ideal inductors used in the design of the matching sections exceeded the maximum values specified in Section 5.5, and since the estimated Q of a practical inductor at 10 GHz is 6, an overall final optimization is required, allowing all inductors a Q of 6 and setting all inductors in excess of 10 nH to this maximum limit. The final result of the overall amplifier optimization routine yields the schematic shown in Figure 5.10.

5.9 Inductor Design

The inductor design is carried out by the expanded Grover method outlined by H. M. Greenhouse;[4] following this method the self inductances of the individual segments of the planar inductor are evaluated; then these self inductances are added to obtain the total self inductance of the coil; next the positive mutual inductances between segments carrying currents of the same phase are evaluated and added to the total self inductance, and finally the negative mutual inductances between segments carrying currents of opposite phase are evaluated and subtracted from the total self inductance, thus obtaining the total inductance of the rectangular inductor.

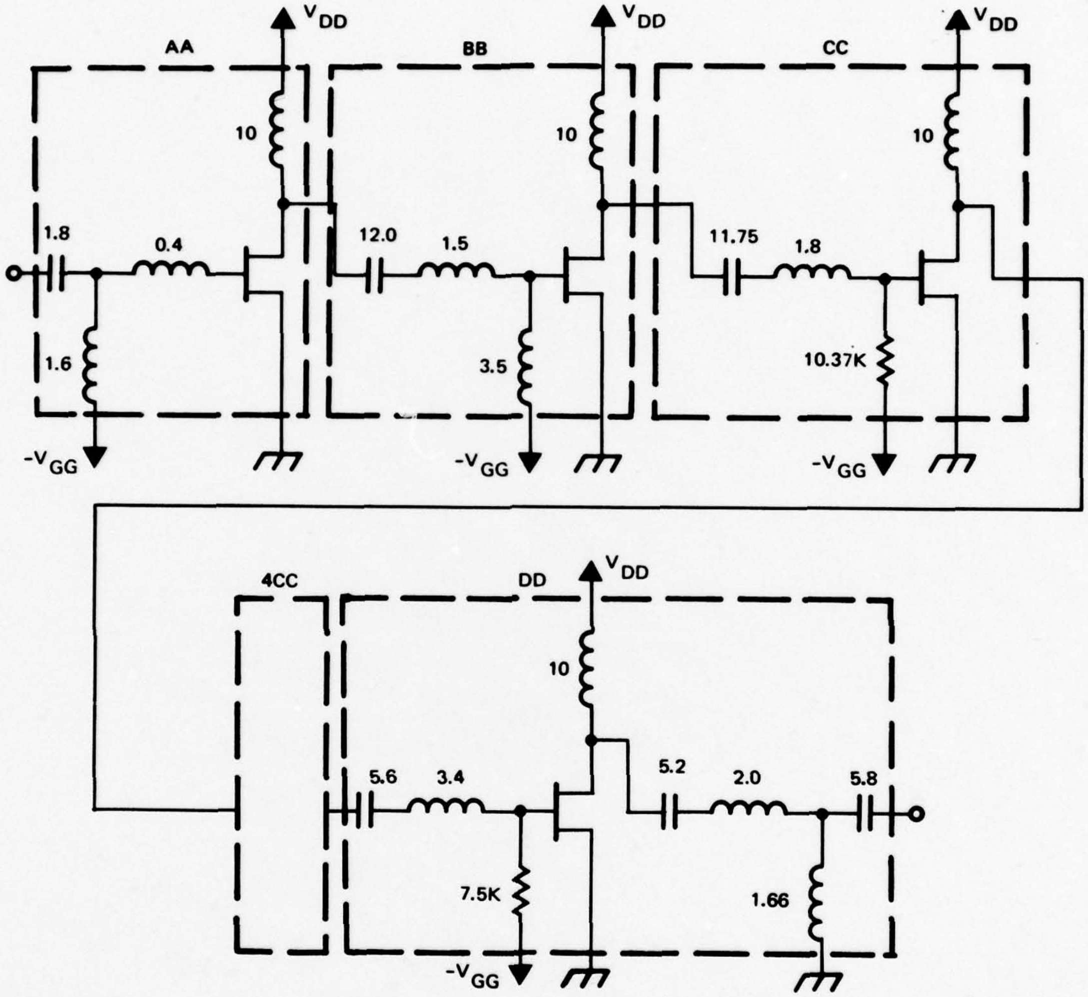
The computer program that carries out this evaluation is attached at the end of this section; this program also extends the calculations to include the associated parasitic capacitance of the inductor to be used in the optimization routine for the amplifier design, if necessary.

6.0 COMPARISON OF PERFORMANCE GOALS AND PREDICTED PERFORMANCE

Computer analysis of the circuit shown in Figure 5.10 gives the following predicted performance results.

	Performance Goals	Predicted Performance
• Gain @ 10 GHz (dB)	30	30.38
• Noise Figure @ 10 GHz (dB)	3.0	3.3
• DC Power (mW)	<500	202
• Frequency Response (GHz)	8 to 11	8 to 11

A plot of the predicted gain and noise figure over the extended range from 6.0 to 13 GHz is shown in Figure 6.1.



- ALL CAPACITOR VALUES ARE IN pF
- ALL INDUCTOR VALUES ARE IN nH
- ALL RESISTOR VALUES ARE IN OHMS

Figure 5.10 Preamplifier schematic diagram

```
100   PRINT"THIS PROGRAM CALCULATES THE INDUCTANCE OF A PLANAR"
110   PRINT"RECTANGULAR MICROELECTRONICS COIL. ALL DIMENSIONS"
120   PRINT"MUST BE GIVEN IN CMS. OPERATING FREQUENCY MUST BE"
130   PRINT"GIVEN IN GHZ. S=INTER-TRACK SPACING. W=TRACK WIDTH"
140   PRINT"T=SEGMENT THICKNESS. RO=METAL RESISTIVITY (OHMS-CM)."
150   PRINT"L1,L2=LENGTHS OF OUTER SEGMENTS. N=NUMBER OF TURNS."
160   PRINT"ENTER S,W,T,L1,L2,N,F,RO"
170   INPUT S,W,T,L1,L2,NO,FO,RO
180   PRINT"S(CMS)=":S:"  W(CMS)=":W:"  T(CMS)=":T
190   PRINT"L1(CMS)=":L1:"  L2(CMS)=":L2:"  N=":NO:"  F(GHZ)=":FO
200   Z=4*NO
210   N=FIX(NO)
220   EO=FIX(Z/2)
230   OO=Z-EO
240   DIM L(Z)
250   DIM G(Z-2,Z)
260   DIM A(Z-2,Z)
270   DIM A$(Z-2,Z)
280   DIM P(Z-2,Z)
290   DIM Q(Z-2,Z)
300   DIM M(Z-2,Z)
310   DIM B(Z-2,Z)
320   DIM C(Z-2,Z)
330   DIM D(Z-2,Z)
340   DIM E(Z-2,Z)
350   DIM F(Z-2,Z)
360   DIM H(Z-2,Z)
370   DIM B$(Z-2,Z)
380   DIM C$(Z-2,Z)
390   DIM D$(Z-2,Z)
400   DIM E$(Z-2,Z)
410   DIM F$(Z-2,Z)
420   DIM H$(Z-2,Z)
430   L(1)=L1
440   L(2)=L2
450   L3=0
460   L4=0
470   S1=2*L1*(LOG(2*L1/(W+T))+0.50049+(W+T)/(3*L1))
480   S2=2*L2*(LOG(2*L2/(W+T))+0.50049+(W+T)/(3*L2))
490   FOR Y1=2 TO Z STEP 1
500   IF Y1>EO THEN 580
510   L(2*Y1)=L2-(Y1-1)*(W+S)
```

```
520    IF L(2*Y1)>0 THEN 560
530    PRINT"DIMENSION L2 INCOMPATIBLE WITH NUMBER OF TURNS,"
540    PRINT"INCREASE IN L2 OR REDUCTION OF TURNS SUGGESTED."
550    GOTO 160
560    L4=L4+L(2*Y1)
570    S2=S2+2*L(2*Y1)*(LOG(2*L(2*Y1)/(W+T))+0.50049+(W+T)/(3*L(2*Y1)))
580    IF Y1>00 THEN 670
590    L(2*Y1-1)=L1-(Y1-2)*(W+S)
600    IF L(2*Y1-1)>0 THEN 640
610    PRINT"DIMENSION L1 INCOMPATIBLE WITH NUMBER OF TURNS,"
620    PRINT"INCREASE IN L1 OR REDUCTION OF TURNS SUGGESTED."
630    GOTO 160
640    L3=L3+L(2*Y1-1)
650    S1=S1+2*L(2*Y1-1)*(LOG(2*L(2*Y1-1)/(W+T))+0.50049+(W+T)/(3*L(2*Y1-1)))
660    NEXT Y1
670    LO=S1+S2
680    L5=L3+L4+L2+L1
690    PRINT "RO(OHMS)=";RO;"   TOTAL LENGTH OF SEGMENTS (CM)=";L5
700    REM  CALCULATION OF MUTUAL INDUCTACE TERMS
710    X=1
720    E1=4*N*(N-1)+2*N*(Z-4*N)
730    YO=Z-4
740    GOTO 770
750    E1=4*N^2+2*N*(Z-4*N)+(Z-4*N-2)*(Z-4*N-1)*(Z-4*N)/3
760    YO=Z-2
770    K=0
780    IO=0
790    FOR J=1 TO N STEP 1
800    FOR Y=1 TO YO STEP 1
810    IF X=0 THEN 840
820    K1=Y+4*J
830    GOTO 850
840    K1=Y+4*J-2
850    IF K1>Z  THEN 1270
860    K=K+1
870    IF K>E1 THEN 1280
880    IF X=0 THEN 910
890    AO=J*(W+S)
900    GOTO 920
910    AO=L(K1-1)+(J-1)*(S+W)
920    A1=AO/W
930    A(Y,K1)=LOG(AO)-1/12/A1^2-1/60/A1^4
```

```
940   A$(Y,K1)=1/168/A1↑6+1/360/A1↑8+1/660/A1↑10
950   G(Y,K1)=EXP(A(Y,K1)-A$(Y,K1))
960   IF X=0 THEN 990
970   Q(Y,K1)=J*(W+S)
980   GOTO 1000
990   Q(Y,K1)=(J-1)*(W+S)
1000   IF Y=1 THEN 1030
1010   P(Y,K1)=J*(W+S)
1020   GOTO 1040
1030   P(Y,K1)=(J-1)*(W+S)
1040   B(Y,K1)=G(Y,K1)/(L(K1)+P(Y,K1))-SQR(1+(G(Y,K1)/(L(K1)+P(Y,K1)))↑2)
1050   C(Y,K1)=LOG((L(K1)+P(Y,K1))/G(Y,K1)+SQR(1+((L(K1)+P(Y,K1))/G(Y,K1))↑2))
1060   D(Y,K1)=2*(L(K1)+P(Y,K1))*(B(Y,K1)+C(Y,K1))
1070   E(Y,K1)=G(Y,K1)/(L(K1)+Q(Y,K1))-SQR(1+(G(Y,K1)/(L(K1)+P(Y,K1)))↑2)
1080   F(Y,K1)=LOG((L(K1)+Q(Y,K1))/G(Y,K1)+SQR(1+((L(K1)+Q(Y,K1))/G(Y,K1))↑2))
1090   H(Y,K1)=2*(L(K1)+Q(Y,K1))*(E(Y,K1)+E(Y,K1))
1100   IF P(Y,K1)=0 THEN 1120
1110   GOTO 1140
1120   B$(Y,K1)=0
1130    GOTO 1150
1140   B$(Y,K1)=G(Y,K1)/P(Y,K1)-SQR(1+(G(Y,K1)/P(Y,K1))↑2)
1150   C$(Y,K1)=LOG(P(Y,K1)/G(Y,K1)+SQR(1+(P(Y,K1)/G(Y,K1))↑2))
1160   D$(Y,K1)=2*P(Y,K1)*(B$(Y,K1)+C$(Y,K1))
1170   IF Q(Y,K1)=0 THEN 1190
1180   GOTO 1210
1190   E$(Y,K1)=0
1200   GOTO 1220
1210   E$(Y,K1)=G(Y,K1)/Q(Y,K1)-SQR(1+(G(Y,K1)/Q(Y,K1))↑2)
1220   F$(Y,K1)=LOG(Q(Y,K1)/G(Y,K1)+SQR(1+(Q(Y,K1)/G(Y,K1))↑2))
1230   H$(Y,K1)=2*Q(Y,K1)*(E$(Y,K1)+F$(Y,K1))
1240   M(Y,K1)=D(Y,K1)+H(Y,K1)-D$(Y,K1)-H$(Y,K1)
1250  IO=IO+M(Y,K1)
1260  NEXT Y
1270  NEXT J
1280 IF X=0 THEN 1320
1290  M1=IO
1300  X=0
1310  GOTO 750
1320  M2=IO
1330  R=RO*L5/W/T
1340  QO=2*PI*FO*(LO+M1-M2)/R
1350  PRINT "LO=";LO;"    M(+)=";M1;"    M(-)=";M2;"  R(OHMS)=";F
```

```
1360  PRINT"L(NH)=":L0+M1-M2:"    Q AT":F0:"GHZ=":Q0
1370  PRINT
1380  PRINT"DO YOU WISH CALCULATION OF PARASITICS2 (1 OR 0)"
1390  INPUT X0
1400  IF X0=0 THEN 1480
1410  E2=8.854E-14
1420  E3=12.5
1430  PRINT"ENTER COIL TO GROUND PLANE SEPARATION (CMS)"
1440  INPUT D0
1450  C1=E3*E2*W*L5/D0
1460  PRINT"COIL TO GROUND PLANE SEPARATION (CMS)=":D0
1470  PRINT"PARASITIC CAPACITANCE TO GROUND FOR GA.AS.(PF)=":C1*1E12
1480  END
```

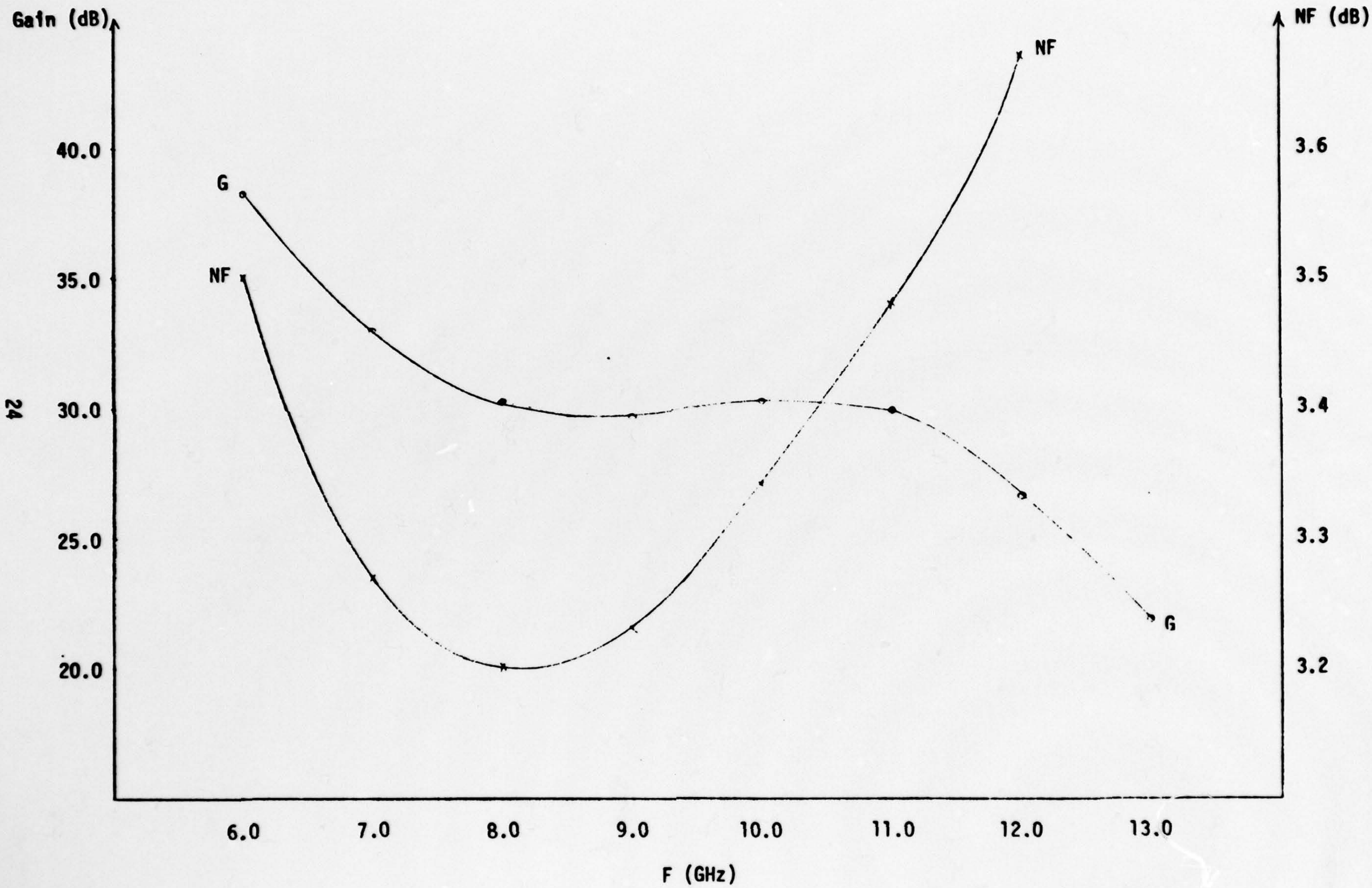


Figure 6.1 Preamplifier's predicted noise and gain performance vs. frequency.

7.0 RF STABILITY ANALYSIS

For the overall amplifier at all frequencies between 100 MHz to 19 GHz $|S_{11}|\leq 1$, $|S_{22}|<1$ and K>1; consequently, the amplifier is unconditionally stable for this frequency range.

8.0 SENSITIVITY ANALYSIS OF PREDICTED PERFORMNACE TO TOLERANCE OF COMPONENT VALUES, GEOMETRY AND CHANNEL DOPING DENSITY

By ofsetting each component type 10% of the nominal value, and all in the same direction, a sensitivity analysis to tolerance of component values was performed with the results shown in Figures 6.2, 6.3 and 6.4, where the component types are resistors, capacitors, and inductors respectively. It can be observed from these figures that inductors are by far the most critical type of component element; consequently, their design needs to be as accurate as possible.

The sensitivity analysis of the predicted performance to tolerances in channel doping density, channel depth, and gate length is shown in Figures 6.5, 6.6, and 6.7, respectively.

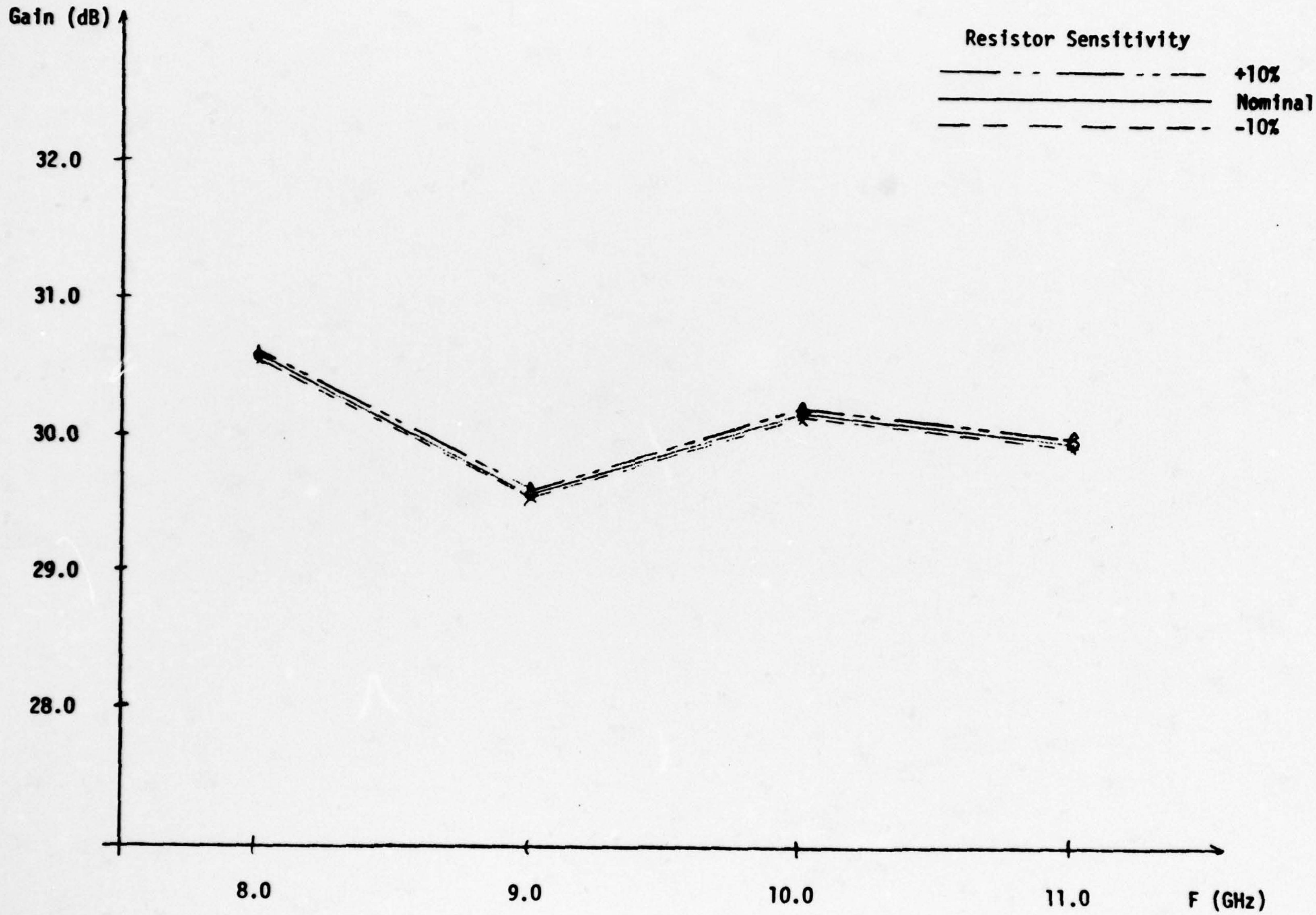


Figure 6.2 Preamplifier's resistor sensitivity vs. frequency.

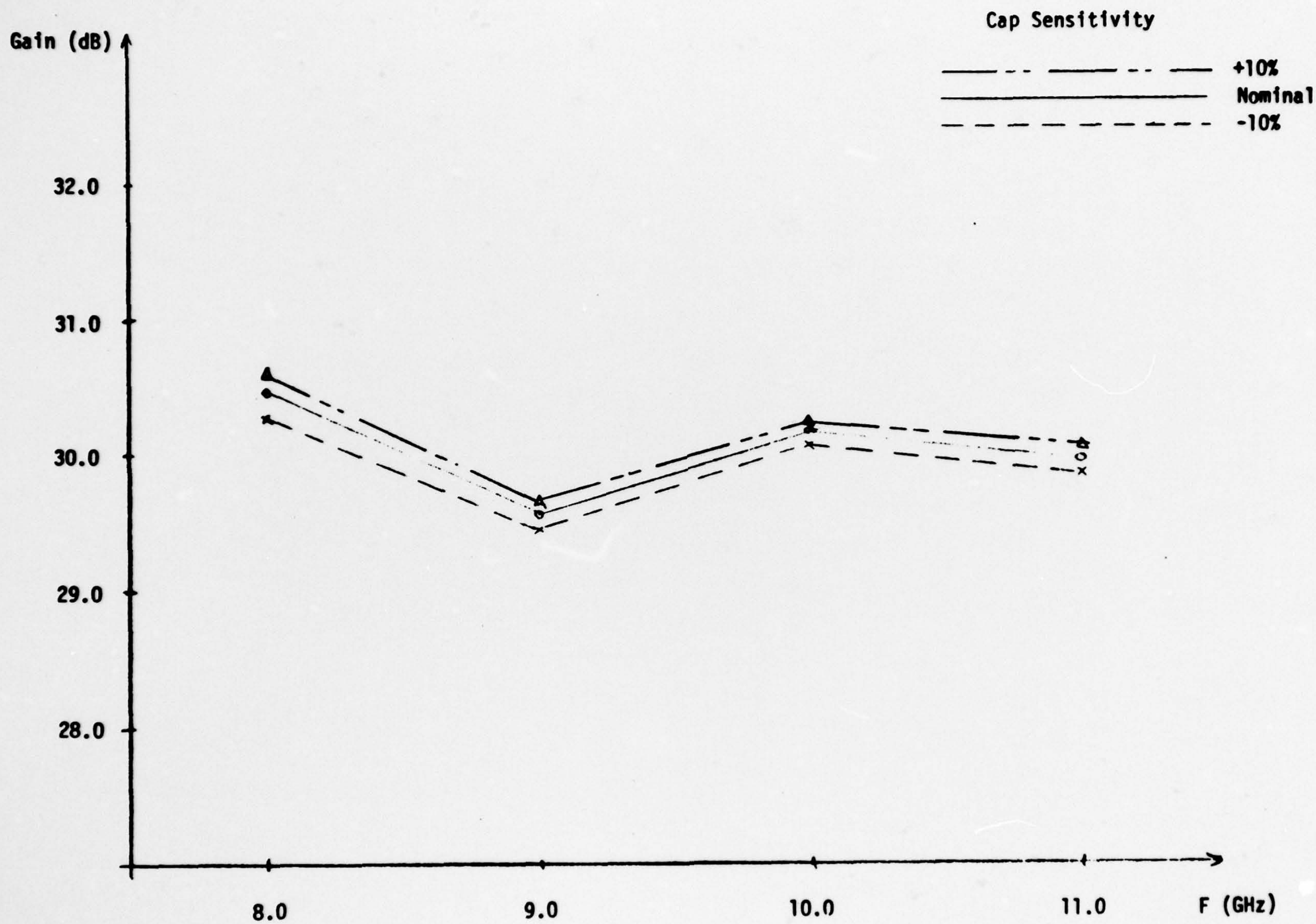


Figure 6.3 Preamplifier's capacitor sensitivity vs. frequency.

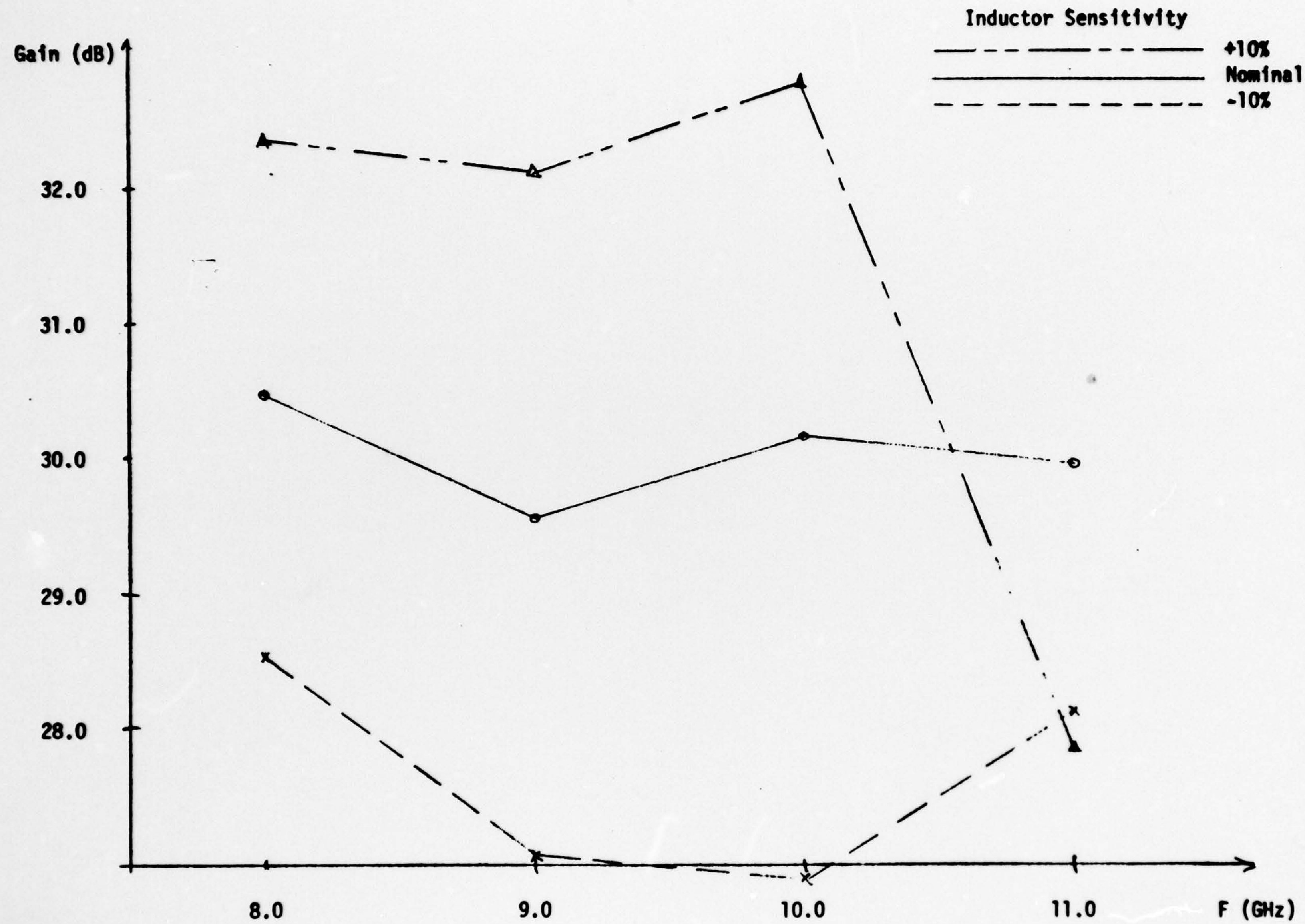


Figure 6.4 Preamplifier's inductor sensitivity vs. frequency.

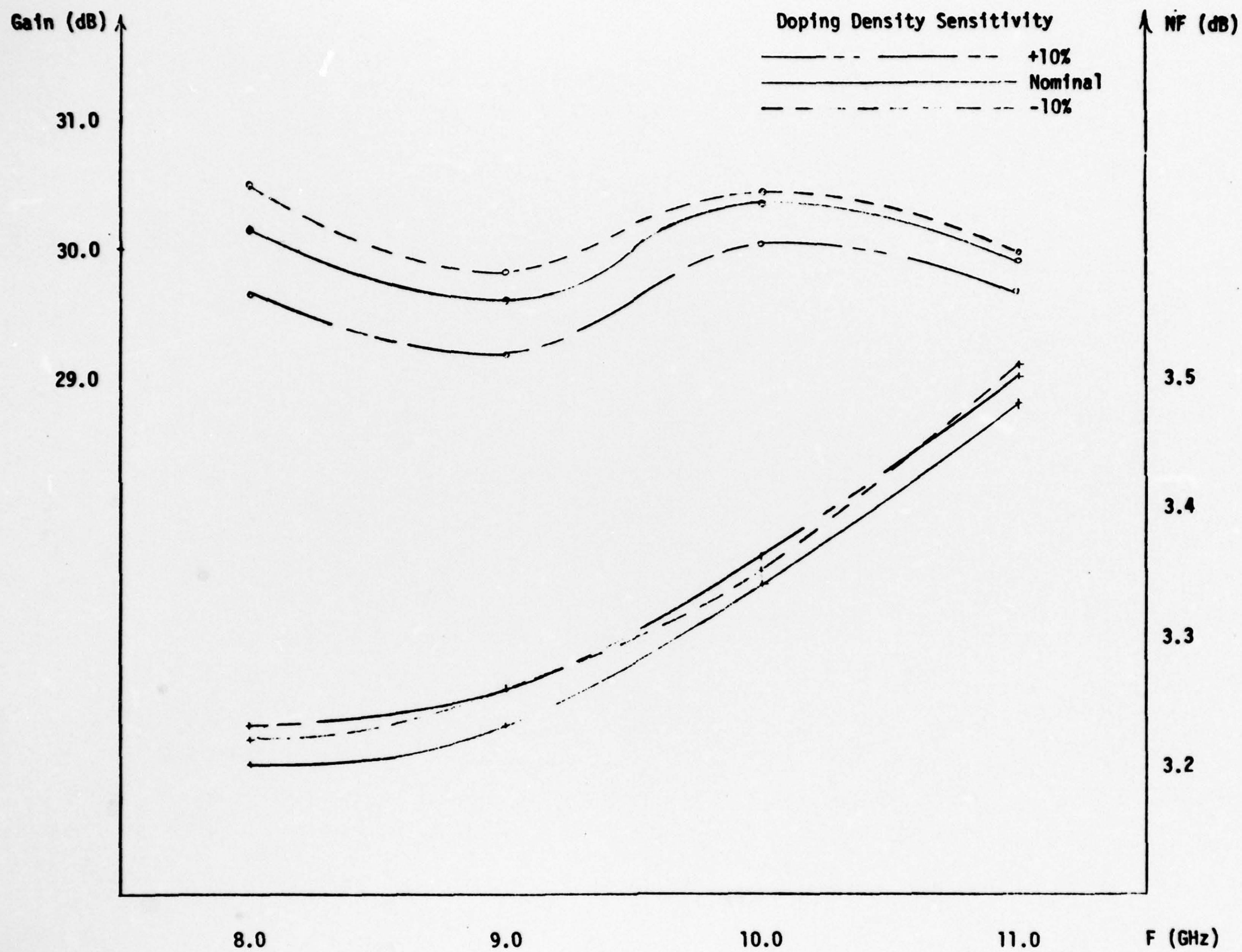


Figure 6.5 Preamplifier's doping density sensitivity vs. frequency.

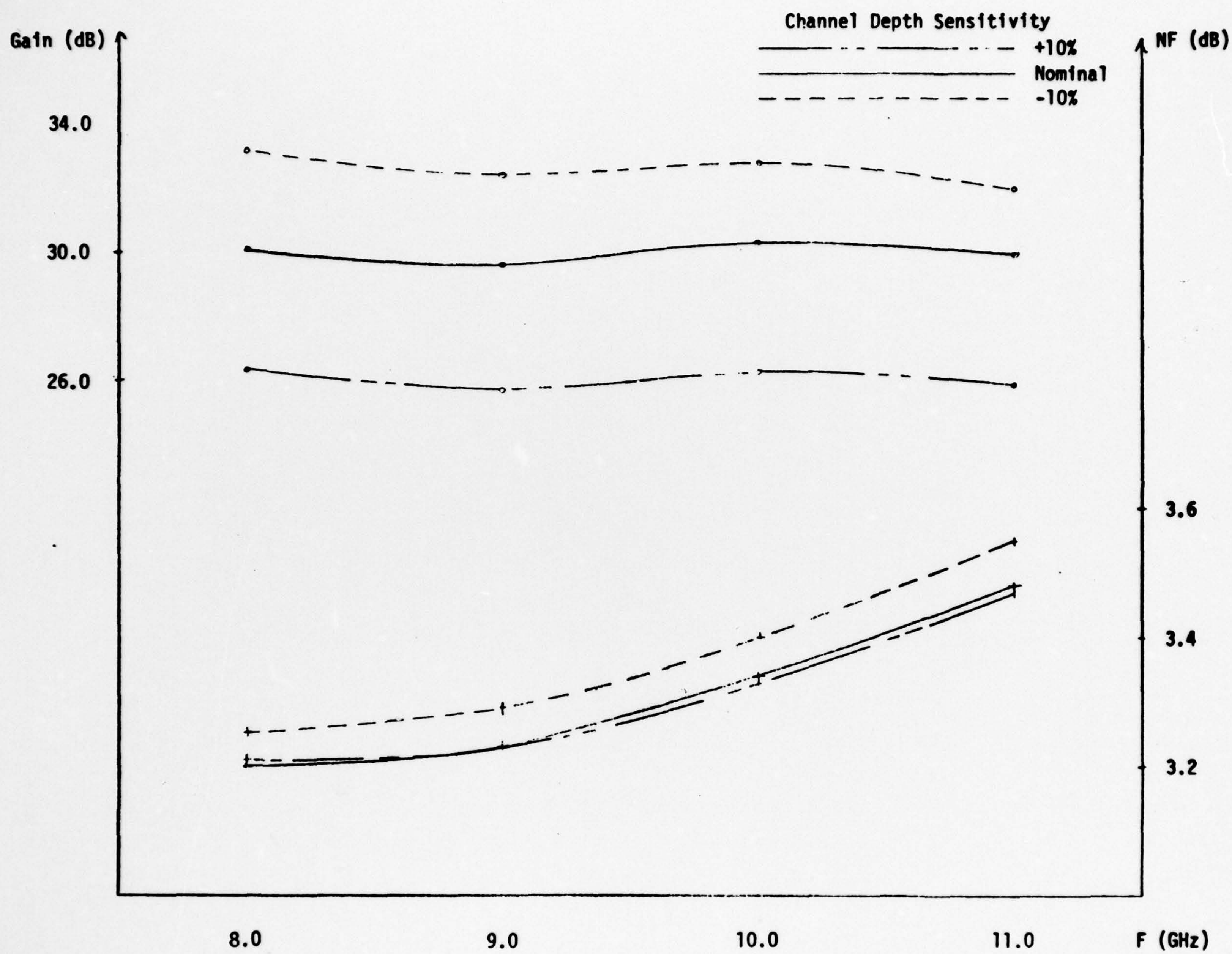


Figure 6.6 Preamplifier's channel depth sensitivity vs. frequency.

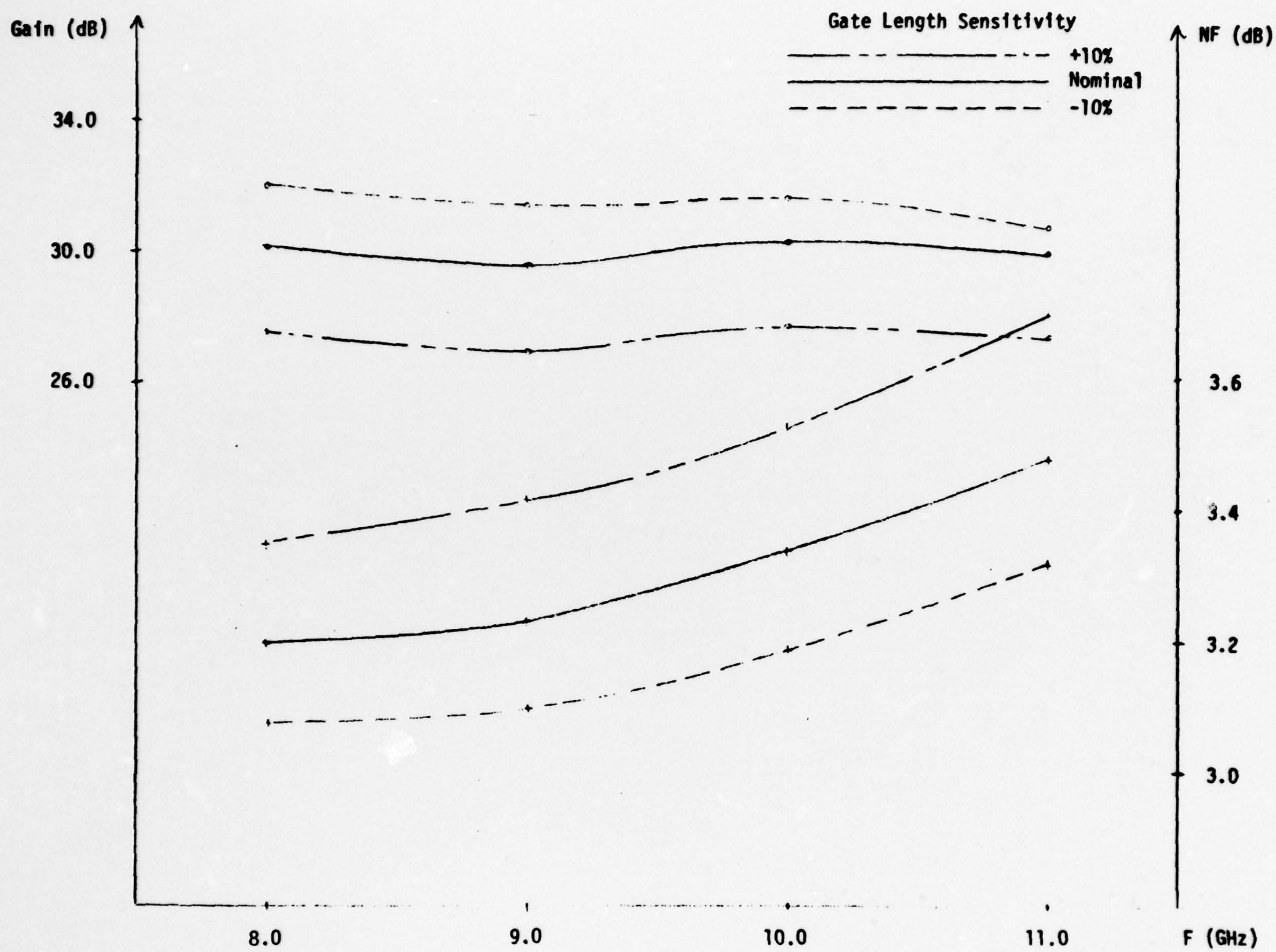


Figure 6.7 Preamplifier's gate length sensitivity vs. frequency.

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